REMARKS/ARGUMENTS

In the Office Action mailed February 19, 2009, claims 1-24 were rejected. Additionally, the drawings were objected to. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are added or canceled.

For reference, claims 1, 9, and 17 are amended. In particular, claim 1 is amended to recite detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test-mode of the self-timed memory. Claims 9 and 17 are each amended to recite similar limitations. These amendments are supported, for example, by the subject matter described in the specification at page 2, lines 6-10, of the present application.

Objections to the Drawings

The Office Action objects to the drawings as needing descriptive labels other than numerical designations for Figs. 3-5. However, it should be noted that the current application is a U.S. National Stage application. The labeling of figures with text matter is prohibited under PCT Rule 11.11, except when absolutely indispensible for understanding. Further, MPEP 1893.03(f) states that "[t]he USPTO may not impose requirements beyond those imposed by the Patent Cooperation Treaty (e.g., PCT Rule 11)." In the present application, Applicants submit that the addition of text labels to the drawings is not "absolutely indispensible" because the individual drawing elements are identified and described in the specification. In view of the above rules, Applicants respectfully assert that additional text labeling is not required in the drawings of the current application.

Claim Rejections under 35 U.S.C. 112, first paragraph

Claims 1, 9, and 17 were rejected under 35 U.S.C. 112, first paragraph, as purportedly failing to comply with the written description requirement. Specifically, the Office Action states:

> The amended limitation "wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal" is not supported by the specification filed August 30, 2006. Applicant is unpersuasive in the citation of page 4, lines 12 – 22. Page 4, lines 12 – 22 discloses an "external control…using the test system" and "the test system implemented for modifying the duty cycle". The cited specification does not disclose the modification of duty cycle of the internal clock signal independent of the duty cycle of the external clock signal. The specification discloses a test system that has the ability to control the duty cycle of the internal clock signal though the modification of the duty cycle of the external clock system, though the functionality of the external controls. Examiner understands that any manipulation of duty cycle for the internal clock signal and external clock signal is performed by the test system, external to the device under test. For purposes of examination the examiner assumes that during a test mode the self-timed memory is powered by an external clock signal.
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> (Underlining added, sic all.)

While the specification may not explicitly provide antecedent basis for the exact language used in the claims, Applicants respectfully submit that the indicated language finds considerable support in the specification, including the support described below. See, MPEP 608.01(o) ("an applicant is not limited to the nomenclature used in the application as filed"). Furthermore, 37 C.F.R. 1.75(d)(1) requires the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable. In other words, support is required, and antecedent basis is simply one way of providing support, but antecedent basis is not the only way to provide support for the limitations of the claim.

Here, although the language of the claims differs somewhat from the actual nomenclature provided in the specification, Applicants respectfully submit that the claim language is nevertheless supported by the specification because the claims recite limitations that are well within the scope of the embodiments described in the specification. Applicants respectfully submit that the limitation related to an external clock signal which has a duty cycle that is different from a duty cycle of an internal clock signal is supported by the specification, even though there may not be explicit antecedent basis for the language. This language is supported by the specification, for example, at least in the subject matter described as follows:

> Provision of a control signal during the test mode allows, for example, testing of a plurality of internal memory blocks using one test system by switching provision of the external clock signal to different internal memory blocks according to a predetermined test pattern. The test circuitry generates an external clock signal according to a predetermined test pattern for detecting delay faults, having, for example, a duty cycle lower or higher than the 50% duty cycle of an internal memory block, and provides it to the test system during test mode.
> Present Application, page 6, lines 22-26 (emphasis added).

For a proper contextual understanding of this reference from the specification, it should be noted that the specification also states:

> Depending upon the control signal state (740), an internal clock signal may be provided to the internal memory block during a normal mode of operation (750) of the self-timed memory or an external clock signal to the internal memory block during a test mode (760) of the self-timed memory.
> Present Application, page 7, lines 6-9 (emphasis added).

Thus, the internal clock signal or the external clock signal is used for the internal memory block, depending on whether the internal memory block is in normal mode or test mode.

While the foregoing descriptions from the present application do not explicitly refer to an external clock signal which has a duty cycle that is different from a duty cycle of an internal clock signal, this description nevertheless provides support for the indicated language of the claim. In particular, this description provides support for the language of the claims because embodiments described in the specification use the external clock signal (during test mode) instead of the internal clock signal (during normal mode), at a different duty cycle other than the typical 50% duty cycle used for the internal memory block.

Therefore, Applicants assert the language of the claims is supported by the specification as filed because the language is within the scope of the written description provided in the specification, and the language does not cause confusion as to the meaning of the claims. Accordingly, Applicants respectfully request that the rejections of claims 1, 9, and 17 under 35 U.S.C. 112, first paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 112, second paragraph

Claims 2-4 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claim 2

In regard to the rejection of claim 2, the Office Action states:

> Regarding claim 2, the language "further providing switching provision" is ambiguous and fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner is unclear if the intended meaning is "a switching provision" or "switching a provision".
> (Emphasis added.)

Applicants submit that the language of claim 2 is not ambiguous and, hence, the rejection of claim 2 should be withdrawn. In particular, the language of claim 2 is not ambiguous within the context of the present application because the specification of the present application describes:

> Provision of a control signal during the test mode allows, for example, testing of a plurality of internal memory blocks using one test system by switching provision of the external clock signal to different internal memory blocks according to a predetermined test pattern. The test circuitry generates an external clock signal according to a predetermined test pattern for detecting delay faults, having, for example, a duty cycle lower or higher than the 50% duty cycle of an internal memory block, and provides it to the test system during test mode.
> Present Application, page 6, lines 22-26 (emphasis added).

Furthermore, the specification of the present application describes:

> Depending upon the control signal state (740), an internal clock signal may be provided to the internal memory block during a normal mode of operation (750) of the self-timed memory or an external clock signal to the internal memory block during a test mode (760) of the self-timed memory.
> Present Application, page 7, lines 6-9 (emphasis added).

While the limitations of the specification are not read into the claims, these descriptions from the specification of the present application provide sufficient contextual understanding to prevent ambiguity as to the meaning of the language "further providing switching provision" recited in claim 2. Accordingly, Applicants respectfully request that the rejection of claim 2 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claims 3 and 4

In regard to the rejections of claims 3 and 4, the Office Action states:

> Regarding claims 3 and 4, the language "duty cycle of the internal memory block" is ambiguous. One of ordinary skill in the art would understand "duty cycle" to be a characteristic of a signal with a periodic or repetitive nature. It is unclear how applicant intends the internal memory block to have a duty cycle. The claim therefor fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(Emphasis added.)

Applicants submit that the language of claims 3 and 4 is not ambiguous and, hence, the rejections of claims 3 and 4 should be withdrawn. In particular, the language of claims 3 and 4 is not ambiguous within the context of the present application because the specification of the present application describes:

> Referring to FIG. 2, a test system 100 according to the invention connected to the 2-to-4 address decoder 125 is shown. The test system 100 includes clock signal input ports 104 and 106 for receiving the internal clock signal PHIX from the clock monitor 152 and the external clock signal CL, respectively. Depending on a control signal received at a control input port 108, a multiplexer 110 provides via output port 102 the internal clock signal 107 (PHIX) or the external clock signal CL to the address decoder 125. Depending on the received control signal, the multiplexer 110 provides the internal clock signal PHIX to the address decoder 125 in normal mode or the external clock signal CL during test mode. Interposing the test system 100 between the clock monitor 152 and the address decoder 125 enables control of the clock cycle of the address decoder 125, by directly applying the external clock signal CL to the address decoder 125 during test mode. Thus, the beginning and the end of the activation and deactivation of the word lines is easily controlled by the external clock signal CL enabling the detection of delay faults. As is evident, the test system is easily extended to cover a plurality of internal

memory blocks that are controlled by the internal memory clock such as sense amplifier, column and bank decoder, pre-charge and discharge circuitry, and input/output latches.

Present Application, page 5, lines 3-18 (emphasis added).

Furthermore, the specification of the present application describes:

> Depending upon the control signal state (740), an internal clock signal may be provided to the internal memory block during a normal mode of operation (750) of the self-timed memory or an external clock signal to the internal memory block during a test mode (760) of the self-timed memory.
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> Present Application, page 7, lines 6-9 (emphasis added).

While the limitations of the specification are not read into the claims, these descriptions from the specification of the present application provide sufficient contextual understanding to draw a relationship between the internal and external clock signals and operation of the internal memory block. Thus, references to the "duty cycle of the internal memory block" should be understood within the context of providing either the internal clock signal (having a 50% duty cycle) or the external clock signal (having a different duty cycle) to the internal memory block. Therefore, the references to the "duty cycle of the internal memory block" merely refer to operating the internal memory block according to the duty cycle corresponding to either the internal clock signal or the external clock signal. Therefore, this description in the specification of the present application prevents ambiguity as to the meaning of the language "duty cycle of the internal memory block" recited in claims 3 and 4. Accordingly, Applicants respectfully request that the rejections of claims 3 and 4 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1-13, 16-20, 23, and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. (U.S. Pat. No. 6,115,836, hereinafter Churchill) in view of Irrinki et al. (U.S. Pat. No. 5,822,228, hereinafter Irrinki). Additionally, claims 14, 15, 21, and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill and Irrinki in view of Choi (U.S. Pat. No. 6,324,115, hereinafter Choi). However,

Applicants respectfully submit that these claims are patentable over Churchill, Irrinki, and Choi for the reasons provided below.

Independent Claim 1

Claim 1 recites "detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory" (emphasis added).

In contrast, the combination of cited references does not teach all of the limitations of the claim because the combination of Churchill and Irrinki does not teach detecting slow-to-rise or slow-to-fall delays, as recited in the claim. In particular, neither Churchill nor Irrinki teaches the indicated limitations.

As explained in Applicants' previous response, Churchill generally relates to test mode features for synchronous and pipelined memories. Churchill, col. 1, lines 23-26. More specifically, Churchill describes a programmable scan interface (see 212 of Fig. 2) which provides a mechanism for programmably altering various signals within static random access memory (SRAM) to improve the observability and characterization of circuitry within the SRAM. Churchill, col. 2, lines 49-52. One of the ways to alter signals within the SRAM includes a test mode that causes internal signals of the device under test to be replaced with external signals. Churchill, col. 3, line 66, through col. 4, line 2. As an example, the test mode may enable the replacement of an internally generated clock pulse signal with an external clock signal. Churchill, col. 4, lines 2-4. The external clock signal can be sent to a memory word line to stress the memory cells in a memory core. Churchill, col. 4, lines 4-9; col. 18, line 51, through col. 19, line 10; also see the line 222 which connects the clock pulse generator 210 to the input register 216 and the output register 218 of Fig. 2.

Although Churchill is generally directed to scan path test mode features for synchronous and pipelined memories, Churchill does not appear to mention detecting slow-to-rise or slow-to-fall delays. In fact, Churchill merely teaches means to disable an output register to monitor directly the effects of internal clock signals on the memory core, as well as means to alter the timing of the internal clock signal to determine whether any failures are the result of improper signal timing or a defective memory core.

Churchill, col. 2, lines 23-28. Furthermore, Churchill addresses rising and falling edges of a clock signal, CLK, with respect to a programmable delay circuit. Churchill, col. 13, lines 24-35. However, the description of the programmable delay circuit does not address detection of slow-to-rise and slow-to-fall delays. Therefore, Churchill does not teach detection of slow-to-rise and slow-to-fall delays, as recited in the claim.

Irrinki does not remedy this lack of teaching by Churchill because Irrinki also fails to teach detection of slow-to-rise and slow-to-fall delays. Irrinki merely describes a built-in self test (BIST) module for determining propagation delay of embedded cores and integrated circuits. Irrinki, col. 1, lines 8-13; col. 2, lines 23-25. The BIST module includes a test generator and a compactor which reside on a chip with a device under test. Irrinki, col. 3, lines 27-29. Under a normal BIST clock configuration, the test generator and comparator use an internal clock source, CLK, to test the general functionality of the device. Irrinki, col. 3, lines 50-56. In order to test the propagation delay of the device, an external clock source, TCLK, is used with variable timing parameters which are changed to gradually decrease the time interval, T_{PD}, between clock edges until a lowest value for which the test results are valid is established and, hence, the measurement of the propagation delay is determined. Irrinki, col. 3, line 57, through col. 4, line 24.

Although Irrinki is generally directed to determining propagation delays of a device under test, Irrinki does not appear to mention detecting slow-to-rise or slow-to-fall delays. In particular, the description of using the internal and external clock sources, CLK and TCLK, to find the lowest value for the time interval, T_{PD}, between clock edges is insufficient to teach detection of slow-to-rise and slow-to-fall delays. Therefore, Irrinki also fails to teach detection of slow-to-rise and slow-to-fall delays, as recited in the claim.

For the reasons presented above, the combination of Churchill and Irrinki does not teach all of the limitations of the claim because neither Churchill nor Irrinki teaches detection of slow-to-rise and slow-to-fall delays, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Churchill and Irrinki because the combination of cited references does not teach all of the limitations of the claim.

Independent Claims 9 and 17

Applicants respectfully assert independent claims 9 and 17 are patentable over the proposed combinations of cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Each of claims 9 and 17 recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of these claims differs from the language of claim 1, and the scope of these claims should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of these claims.

Dependent Claims

Claims 2-8, 10-16, and 18-24 depend from and incorporate all of the limitations of the corresponding independent claims 1, 9, and 17. Applicants respectfully assert claims 2-8, 10-16, and 18-24 are allowable based on allowable base claims. Additionally, each of claims 2-8, 10-16, and 18-24 may be allowable for further reasons, as described below.

Dependent Claim 2

In regard to claim 2, Applicants respectfully submit that claim 2 is patentable over the combination of Churchill and Irrinki because the combination of cited references does not teach all of the limitations of the claim. Claim 2 recites:

> A method for providing an external clock signal to an internal memory block of a self-timed memory as defined in claim 1 further comprising switching provision of the external clock signal received during test mode to different internal memory blocks according to a predetermined test pattern.
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> (Emphasis added.)

It should be noted that the Office Action relies on Churchill as purportedly teaching the indicated language of the claim. The Office Action does not rely on Irrinki for teachings related to switching provision of the external clock signal received during test mode to different internal memory blocks according to a predetermined test pattern.

Although the Office Action relies on Churchill as purportedly teaching the indicated language of the claim, the cited portions of Churchill (col. 18, lines 46-48, and col. 19, lines 5-10) does not address switching provision of the external clock signal received during test mode to different internal memory blocks according to a predetermined test pattern. In fact, neither of these citations relates to providing an external clock signal to different internal memory blocks according to a predetermined pattern. Although the general description which includes the cited portions of Churchill relates to using an external clock signal which has a larger pulse width than that generated internally by a clock pulse generator, this description is insufficient to teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim.

For the reasons presented above, the combination of Churchill and Irrinki does not teach all of the limitations of the claim because neither Churchill nor Irrinki teaches detection of slow-to-rise and slow-to-fall delays, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Churchill and Irrinki because the combination of cited references does not teach all of the limitations of the claim.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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Date: May 19, 2009

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